Remarks

Favorable consideration of the application is respectfully requested. Claims 1-6, prior to this response were pending in the present application. By this paper, claims 1 - 3 and 5 are amended.

Claim Rejections - 35 U.S.C. §103

Claims 1 - 6, prior to this paper, were rejected under 35 U.S.C. §103(a) as being unpatentable over Nishioka et al. (US 5,994,733) in view of Shin et al. (US 2005/0023600 A1).

Claims 1 -3 and 5 have been amended as indicated which further distinguishes the present invention from Nishioka et al. in view of Shin et al.

For example, a portion of claim 1 now reads:

"performing a via etch through the planarized insulation material to completely clear the planarized insulation material residing between the transistor gates, thus exposing ~~expose~~ the etch stop barrier layer and forming rows of source line vias running in the X direction and separate drain vias unique to each transistor running in the Y direction;

clearing a horizontal component of the conformal etch stop barrier layer that covers the source regions and drain regions; and

forming individual drain contacts to a respective transistor gate and rows of source contact interconnects, wherein the individual drain contacts and the rows of source contact interconnects substantially fill openings between the transistor gates and abut to a

vertical component of the conformal etch stop barrier layer residing on the transistor gates."

Claims 2, 3 and 5 have been amended in like manner and address distinct features discussed concerning claim 1. Support is taken from FIG. 6 and 7 and paragraphs 0030 and 0031 of the instant application.

The combination of Nishioka et al. in view of Shin et al. is not applicable in light of the amendment to base claims 1 – 3 and 5 as demonstrated in the following discussion.

Nishioka et al. teaches forming source and drain vias to make contact with the source and drain regions. Nishioka et al. further shows the presence of spacers and a cap formed on the transistor gates. Nishioka et al, however is silent on how transistor spacers and cap were formed or of what material they were formed from (please see Fig. 17B-19B and col 15, lines 1-25).

Shin et al. discloses a method to form source and drain vias that contact the source and drain regions while leaving dielectric material between the transistor gates during the via opening etch (please refer to Fig. 21B-22B and paragraphs 0119-0121).

However, the combination of Nishioka et al. in view of Shin et al. does not teach the processing steps of:

"...performing a via etch through the planarized insulation material to completely clear the planarized insulation material residing between the transistor gates, thus exposing the etch stop barrier layer...

clearing a horizontal component of the conformal etch stop barrier layer that covers the source regions and drain regions...

...wherein the individual drain contacts and the rows of source contact interconnects substantially fill openings between the transistor gates and abut to a vertical component of the conformal etch stop barrier layer residing on the transistor gates..."

The above steps are features of the present invention as relied on for amendment to the claims.

The present invention, as currently amended, is distinct from the teachings of Nishioka et al. in view of Shin et al. in that the presently claimed invention requires that a conformal etch stop layer is formed that covers the transistor gates, followed by a planarized insulation layer that covers the transistor gates. An etch is used to completely remove the insulation material between the transistor gates and to expose the conformal etch stop layer. A following etch removes the horizontal component of the conformal etch stop layer to expose the underlying source and drain implants. Then a source and drain contact of conductive material fills the via openings and abuts to a vertical component of the conformal etch stop layer.

Thus, it is believed that claims 1 – 6, as presently presented, are patentable over the art of record and in particular over Nishioka et al. (US 5,994,733) in view of Shin et al. (US 2005/0023600 A1).

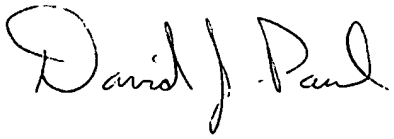
Therefore, by amendment and by the reasons presented, the rejection of claims 1 - 6, under 35 U.S.C. §103(a) as being unpatentable over Nishioka et al. (US 5,994,733) in view of Shin et al. (US 2005/0023600 A1) is overcome.

Conclusion

Applicant submits that the application is in condition for allowance. Such allowance at an early date is respectfully requested.

To that end, if the Examiner feels that a conference will expedite the prosecution of this case, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,



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